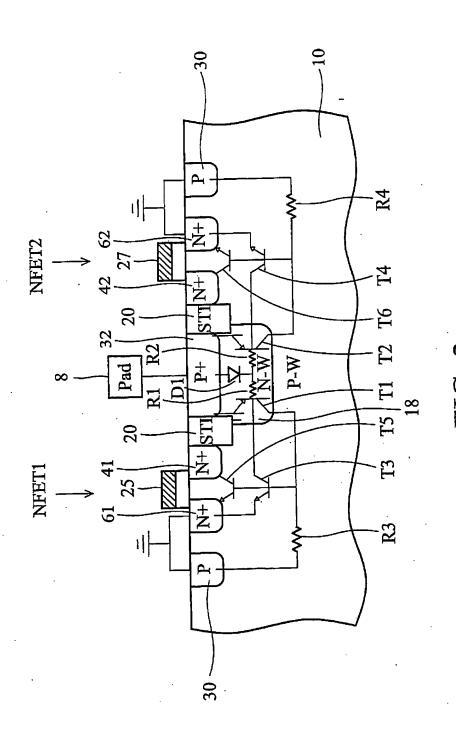


FIG. 1 (Prior Art)



Creating a N-well within a semiconductor substrate Creating multiple ST1 structures within the semiconductor substrate bridging the N-well substrate boundary at the surface region Creating poly gate elements on the substrate surface Creating N+ source-drain areas within the substrate on either side of the poly gate elements forming NFET elements Creating q P+ contact region within the N-well and creating P+ regions in the substrate outside of the N-well region Crating a first and second electrical conductor system Connecting the N-well P+ contact with the first conductor system to a first voltage source, the active circuit signal input pad Connecting the NFET N+ source and the substrate P+ contact areas with the second conductor system to a second woltage source, typically ground Allowing the NFET gates and drain elements to be electrically floating Creating a passivation layer for the protection device

FIG. 4

,8

FIG. 5D

BEST AVAILABLE COPY

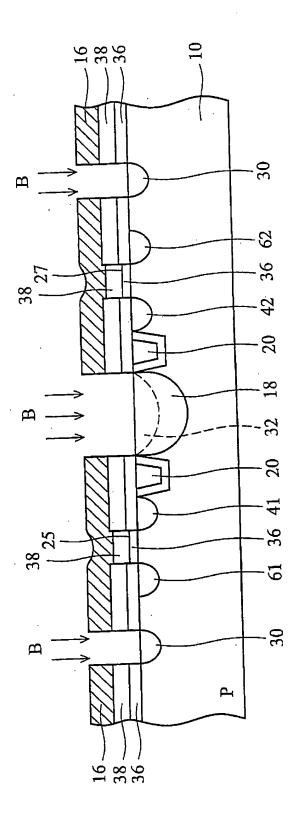


FIG. 5E